We claim:

1 1. A method, comprising:

2 providing at least three elements, including a first element and a last element, each

3 element having an associated parameter;

4 providing a first identifier for the first element;

5 for a first sequential execution of the at least three elements, performing a first operation

6 on the first identifier and at least one of the parameters to produce a transform;

7 saving the transform; and

8 for a second sequential execution of the elements, performing a second operation on the

9 transform to produce a last identifier associated with the last element.

1 2. The method of claim 1, wherein performing the first operation includes:

2 performing a first logic function on the first identifier and the parameter associated with

3 the first element to produce a next identifier for a next one of the elements;

4 repeating the performing a first logic function on the next identifier and the parameter

5 associated with the next one of the elements, until a last identifier has been

6 produced that is associated with the last element; and

7 performing a second logic function on the first identifier and the last identifier to produce

8 the transform.

1 3. The method of claim 2, wherein performing the first logic function includes:

2 shifting the first identifier to produce a shifted identifier; and

3 performing an exclusive OR operation on the shifted identifier and the associated

4 parameter to produce the next identifier.

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1   4.   The method of claim 3, wherein shifting the first identifier includes shifting the first

2   identifier one bit to the left relative to the associated parameter.

1   5.   The method of claim 2, wherein performing the second logic function includes:

2   shifting the first identifier to produce a shifted identifier; and

3   performing an exclusive OR operation on the shifted identifier and the last identifier to

4   produce the transform.

1   6.   The method of claim 5, wherein shifting the first identifier includes shifting the first

2   identifier to the left relative to the last identifier by a number of bits equal in value to one less

3   than a quantity of the at least three elements.

1   7.   The method of claim 1, wherein performing the second operation includes:

2   shifting the first identifier to produce a shifted identifier; and

3   performing an exclusive OR operation on the shifted identifier and the transform to

4   produce the last identifier.

1   8.   The method of claim 7, wherein shifting the first identifier includes shifting the first

2   identifier to the left relative to the transform by a number of bits equal in value to one less than a

3   quantity of the at least three elements.

1   9.   The method of claim 1, wherein the at least three elements are branch instructions in an

2   instruction execution pipeline.

1   10.   The method of claim 1, further comprising:

2   using the last index to access a location in a prediction array; and

3   using a content of said location to predict a decision status of the last element.

1   11.   A circuit, comprising:

2   first and second exclusive OR circuits;

3   a first register having an output coupled to a first input of the first exclusive OR circuit

4   and having an input coupled to an output of the first exclusive OR circuit;

5   a second register having an output coupled to a first input of the second exclusive OR

6   circuit and having an input;

7   a multiplexer having an output coupled to the input of the second register, having a first

8   input coupled to the output of the first exclusive OR circuit, and having a second

9   input coupled to the output of the second register;

10   wherein the output of the first exclusive OR circuit is coupled to a second input of the

11   second exclusive OR circuit.

1   12.   The circuit of claim 11, wherein the first input of the first exclusive OR circuit is offset

2   from the output of the first register to perform a bit-shift operation on data received from the first

3   register by the first exclusive OR circuit.

1   13.   The circuit of claim 11, wherein the second input of the multiplexer is offset from the

2   output of the second register to perform a bit-shift operation on data received from the second

3   register by the multiplexer.

1   14.   The circuit of claim 11, further comprising an array coupled to an output of the second

2   exclusive OR circuit to store transforms generated by the second exclusive OR circuit.

1   15.   The circuit of claim 14, further comprising a counter to generate a shift value to store in

2   the array.

1   16.   A computer system, comprising:

2   an instruction execution pipeline; and

3   a branch prediction circuit coupled to the instruction execution pipeline and including:

4   first and second exclusive OR circuits;

5   a first register having an output coupled to a first input of the first exclusive OR

6   circuit and having an input coupled to an output of the first exclusive OR

7   circuit;

8   a second register having an output coupled to a first input of the second exclusive

9   OR circuit and having an input; and

10   a multiplexer having an output coupled to the input of the second register, having

11   a first input coupled to the output of the first exclusive OR circuit, and

12   having a second input coupled to the output of the second register;

13   wherein the output of the first exclusive OR circuit is coupled to a second input of

14   the second exclusive OR circuit.

1   17.   The computer system of claim 16, wherein the first input of the first exclusive OR circuit

2   is offset from the output of the first register to perform a bit-shift operation on data received from

3   the first register by the first exclusive OR circuit.

1   18.   The computer system of claim 16, wherein the second input of the multiplexer is offset

2   from the output of the second register to perform a bit-shift operation on data received from the

3   second register by the multiplexer.

1   19.   The computer system of claim 16, further comprising an array coupled to an output of the

2   second exclusive OR circuit to store transforms generated by the second exclusive OR circuit.

1　20.　The computer system of claim 19, further comprising a counter to generate a shift value
2　to store in the array.

1　21.　A circuit, comprising:
2　　　　a register;
3　　　　a data shifting circuit having an input coupled to an output of the register;
4　　　　an exclusive OR circuit having a first input coupled to an output of the data shifting
5　　　　　　circuit;
6　　　　an array coupled to a second input of the exclusive OR circuit to transfer transform data
7　　　　　　to the exclusive OR circuit, and further coupled to the data shifting circuit to
8　　　　　　transfer data shift information to the data shifting circuit; and
9　　　　a prediction logic circuit coupled to an output of the exclusive OR circuit.

1　22.　The circuit of claim 21, further comprising a multiplexer having:
2　　　　an output coupled to an input of the register;
3　　　　a first input to receive initial data; and
4　　　　a second input coupled to the output of the exclusive OR circuit.

1　23.　The circuit of claim 21, wherein the data shifting circuit includes a plurality of inputs
2　coupled to the output of the register to shift data from the register by a selected number of bits.

1　24.　A computer system comprising:
2　　　　an instruction execution pipeline;
3　　　　a transform generation circuit coupled to the instruction execution pipeline and including:
4　　　　　　a register;
5　　　　　　a data shifting circuit having an input coupled to an output of the register;

6   an exclusive OR circuit having a first input coupled to an output of the data

7   shifting circuit;

8   an array coupled to a second input of the exclusive OR circuit to transfer

9   transform data to the exclusive OR circuit, and further coupled to the data

10   shifting circuit to transfer data shift information to the data shifting circuit;

11   and

12   a prediction logic circuit coupled to an output of the exclusive OR circuit.

1   25.   The computer system of claim 24, further comprising a multiplexer having:

2   an output coupled to an input of the register;

3   a first input to receive initial data; and

4   a second input coupled to the output of the exclusive OR circuit.

1   26.   The computer system of claim 24, wherein the data shifting circuit includes a plurality of

2   inputs coupled to the output of the register to shift data from the register by a selected number of

3   bits.

1   27.   A machine-readable medium having stored thereon instructions, which when executed by

2   at least one processor cause said at least one processor to perform:

3   providing at least three elements, including a first element and a last element, each

4   element having an associated parameter;

5   providing a first identifier for the first element;

6   for a first sequential execution of the at least three elements, performing a first operation

7   on the first identifier and at least one of the parameters to produce a transform;

8   saving the transform;

9   for a second sequential execution of the elements, performing a second operation on the

10   transform to produce a last identifier associated with the last element;

11   using the last identifier to access a location in a prediction array; and

12   using a content of said location to predict a decision status of the last element.